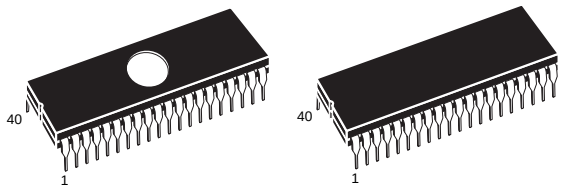
M27W402

4 Mbit (256Kb x16) Low Voltage UV EPROM and OTP EPROM

- 2.7V to 3.6V SUPPLY VOLTAGE in READ OPERATION
- ACCESS TIME:
  - 80ns at V_{CC} = 3.0V to 3.6V
  - 100ns at V_{CC} = 2.7V to 3.6V
- PIN COMPATIBLE with M27C4002
- LOW POWER CONSUMPTION:
  - 15µA max Standby Current
  - 15mA max Active Current at 5MHz
- PROGRAMMING TIME 100µs/word
- HIGH RELIABILITY CMOS TECHNOLOGY
  - 2,000V ESD Protection
  - 200mA Latchup Protection Immunity
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code: 0044h

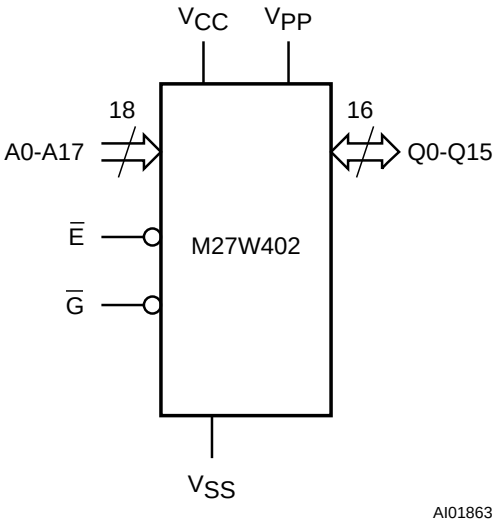


FDIP40W (F) PDIP40 (B)



PLCC44 (K) TSOP40 (N)
10 x 20 mm

Figure 1. Logic Diagram



DESCRIPTION

The M27W402 is a low voltage 4 Mbit EPROM offered in the two range UV (Ultra Violet Erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage and is organised as 262,144 by 16 bits.

The M27W402 operates in the read mode with a supply voltage as low as 2.7V at –40 to 85°C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

The FDIP40W (window ceramic frit-seal package) has a transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27W402 is offered in PDIP40, PLCC44 and TSOP40 (10 x 20 mm) packages.

Figure 2A. DIP Connections

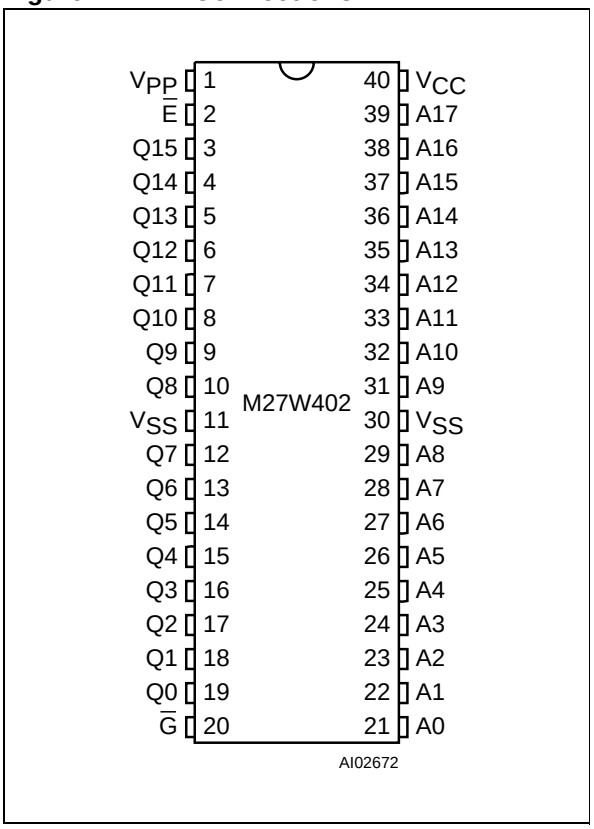


Figure 2B. LCC Connections

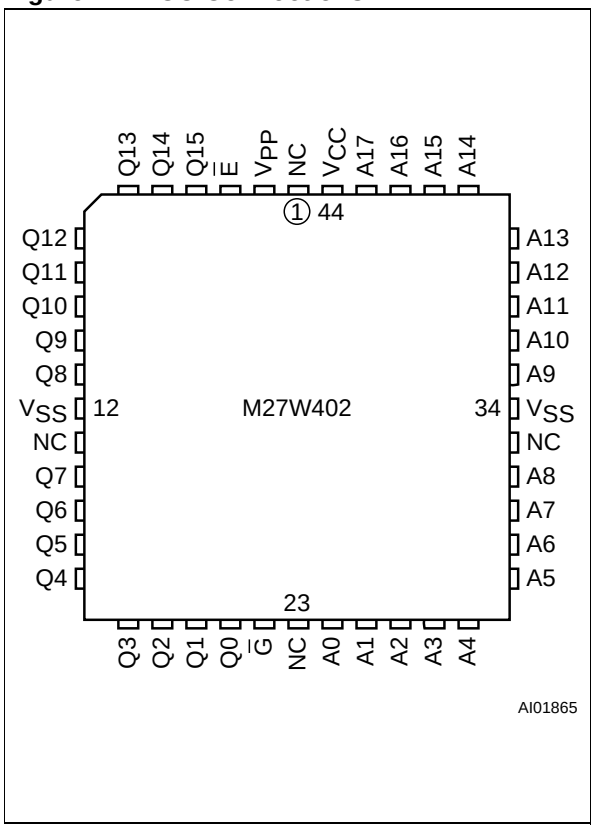


Figure 2C. TSOP Connections

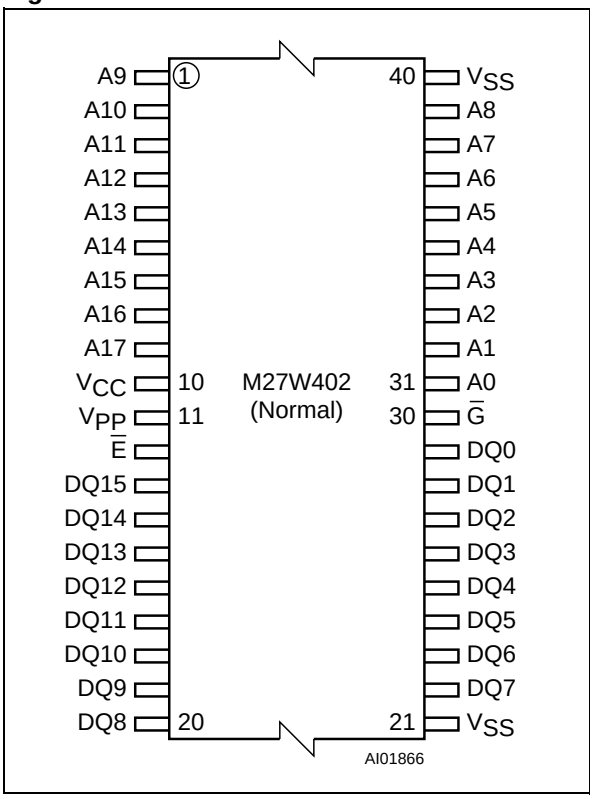


Table 1. Signal Names

A0-A17	Address Inputs
Q0-Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltage (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.
3. Depends on range.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q15-Q0
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	1	0	0	44h

Note: Outputs Q15-Q8 are set to '0'.

Table 5. AC Measurement Conditions

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

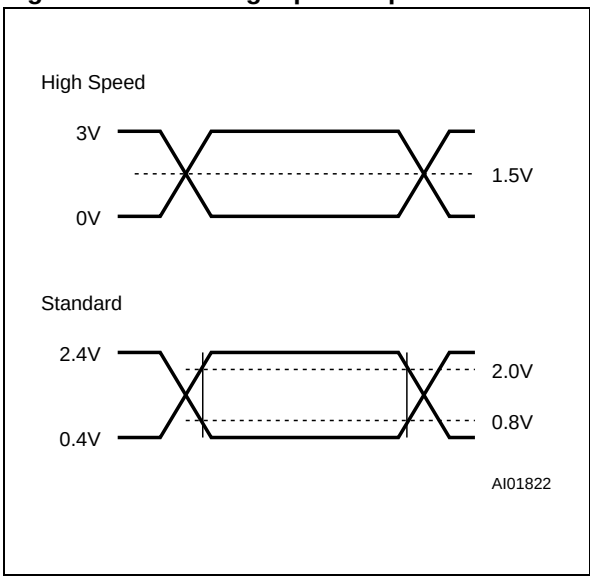


Figure 4. AC Testing Load Circuit

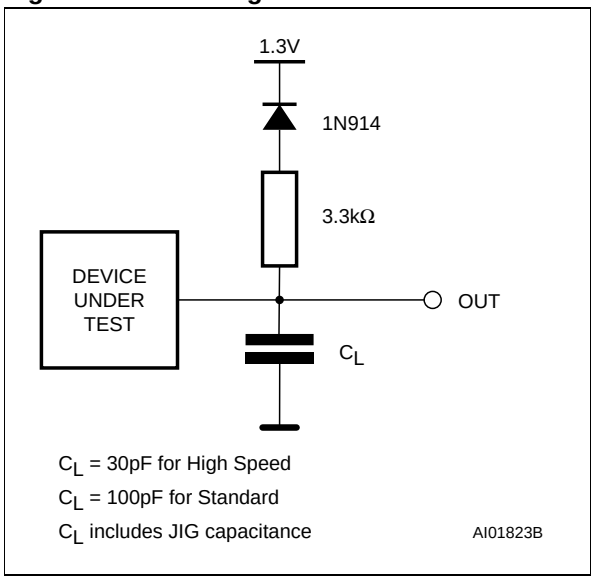


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

DEVICE OPERATION

The operation modes of the M27W402 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27W402 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27W402 has a standby mode which reduces the supply current from 15mA to 15µA with low voltage operation $V_{CC} \leq 3.6V$, see Read Mode DC Characteristics table for details. The M27W402 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 7. Read Mode DC Characteristics (1)
(T_A = –40 to 85°C; V_{CC} = 2.7V to 3.6V; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz, $V_{CC} \le 3.6V$		15	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$, $V_{CC} \le 3.6V$		15	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.6	0.2 V_{CC}	V
V_{IH} (2)	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection.

The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 8. Read Mode AC Characteristics (1)
(T_A = –40 to 85°C; V_{CC} = 2.7V to 3.6V; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27W402						Unit
				-100 (3)				-120 (-150/-200)		
				V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V to 3.6V		V_{CC} = 2.7V to 3.6V		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	0	70	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	0	70	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.
3. Speed obtained with High Speed AC measurement conditions.

Figure 5. Read Mode AC Waveforms

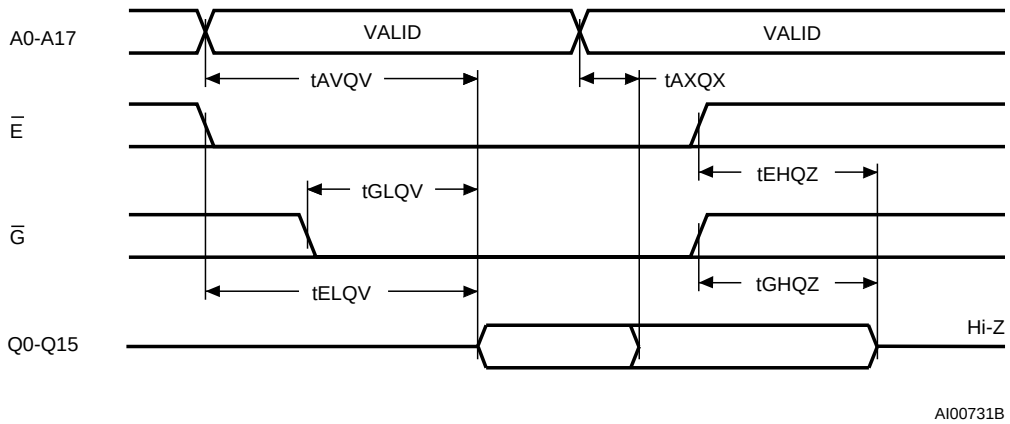


Table 9. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Programming

The M27W402 has been designed to be fully compatible with the M27C4002 and has the same electronic signature. As a result the M27W402 can be programmed as the M27C4002 on the same programming equipment applying 12.75V on V_{PP} and 6.25V on V_{CC} by the use of the same PRESTO II algorithm. When delivered (and after each ‘1’s erasure for UV EPROM), all bits of the M27W402 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a ‘0’ to a ‘1’ by die exposure to ultraviolet light (UV EPROM). The M27W402 is in the programming mode when V_{PP} input is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 6. Programming and Verify Modes AC Waveforms

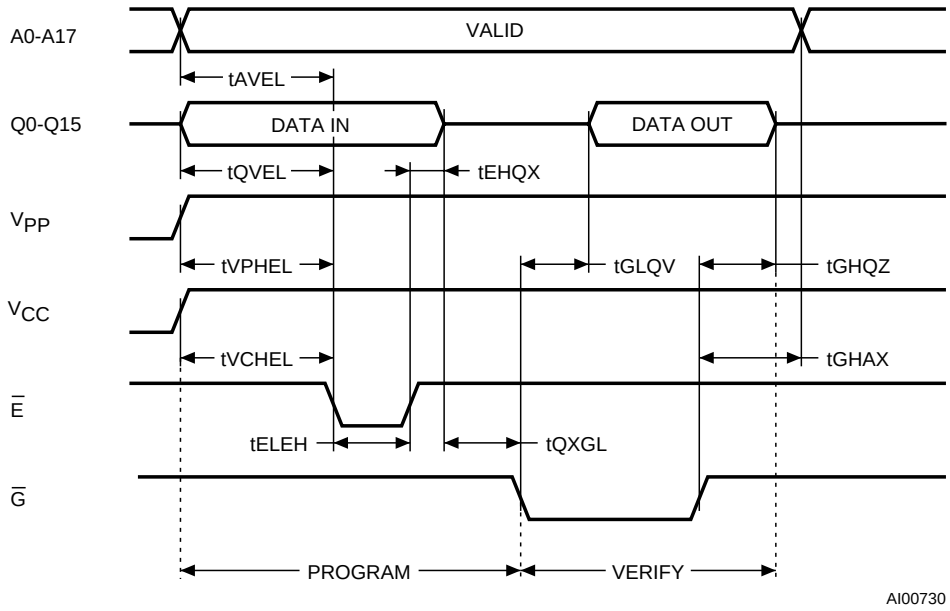
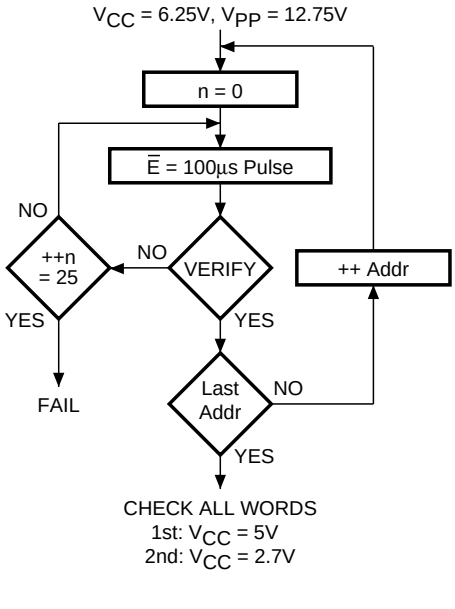


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 26.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs (see Figure 7). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE at V_{CC} much higher than 3.6V, provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27W402s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27W402 may be common. A TTL low level pulse applied to a M27W402's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27W402. A high level $\overline{E}$ input inhibits the other M27W402s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

On-Board Programming

The M27W402 can be directly programmed in the application circuit. See the relevant Application Note AN620.

Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27W402. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27W402 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the STMicroelectronics M27W402, these two identifier bytes are given in Table 4 and can be read-out on outputs Q7 to Q0.

Note that the M27W402 and M27C4002 have the same identifier bytes.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27W402 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27W402 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27W402 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27W402 window to prevent unintentional erasure. The recommended erasure procedure for the M27W402 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27W402 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 11. Ordering Information Scheme

Example: M27W402 -100 K 6 TR

Device Type
M27

Supply Voltage
W = 2.7V to 3.6V

Device Function
402 = 4 Mbit (256Kb x16)

Speed
-100 (1,2) = 100 ns
-120 = 120 ns

Not For New Design (3)
-150 = 150 ns
-200 = 200 ns

Package
F = FDIP40W (4)
B = PDIP40
K = PLCC44
N = TSOP40: 10 x 20 mm (4)

Temperature Range
6 = –40 to 85 °C

Options
TR = Tape & Reel Packing

Note: 1. High Speed, see AC Characteristics section for further information.
2. This speed also guarantees 80ns access time at V_{CC} = 3.0V to 3.6V.
3. These speeds are replaced by the 120ns.
4. Packages option available on request. Please contact STMicroelectronics local Sales Office.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

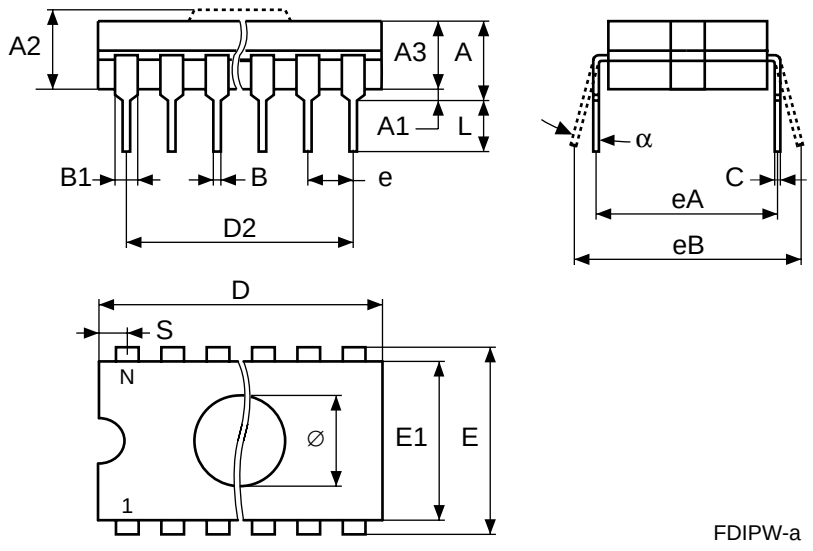
Table 12. Revision History

Date	Revision Details
July 1999	First Issue
03/15/00	FDIP42W Package Dimension, L Max added (Table 13) TSOP40 Package Dimension changed (Table 16) 0 to 70°C Temperature Range deleted Programming Time changed

Table 13. FDIP40W - 40 pin Ceramic Frit-seal DIP with window, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.72			0.225
A1		0.51	1.40		0.020	0.055
A2		3.91	4.57		0.154	0.180
A3		3.89	4.50		0.153	0.177
B		0.41	0.56		0.016	0.022
B1	1.45	–	–	0.057	–	–
C		0.23	0.30		0.009	0.012
D		51.79	52.60		2.039	2.071
D2	48.26	–	–	1.900	–	–
E	15.24	–	–	0.600	–	–
E1		13.06	13.36		0.514	0.526
e	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		16.18	18.03		0.637	0.710
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.62	–	–	0.300	–	–
α		4°	11°		4°	11°
N	40			40		

Figure 8. FDIP40W - 40 pin Ceramic Frit-seal DIP with window, Package Outline

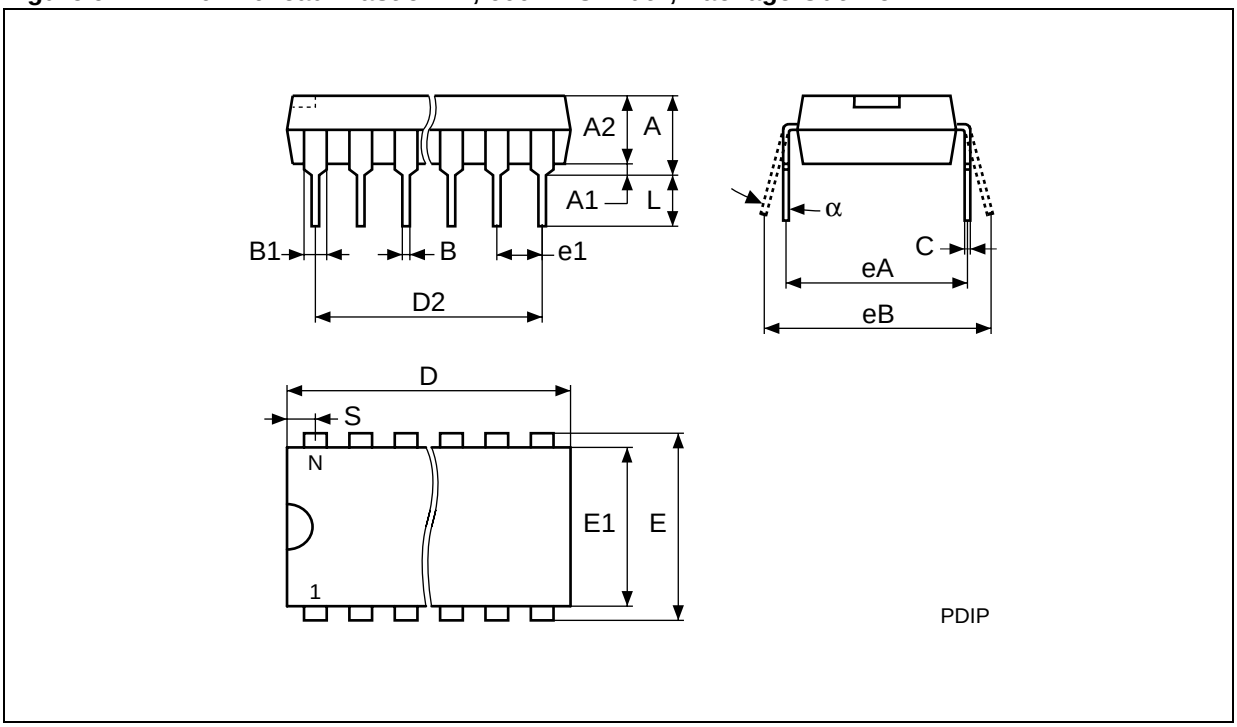


Drawing is not to scale.

Table 14. PDIP40 - 40 pin Plastic DIP, 600 mils width, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	4.45	–	–	0.175	–	–
A1	0.64	0.38	–	0.025	0.015	–
A2		3.56	3.91		0.140	0.154
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		51.78	52.58		2.039	2.070
D2	48.26	–	–	1.900	–	–
E		14.80	16.26		0.583	0.640
E1		13.46	13.99		0.530	0.551
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	
eB		15.24	17.78		0.600	0.700
L		3.05	3.81		0.120	0.150
S		1.52	2.29		0.060	0.090
α		0°	15°		0°	15°
N	40			40		

Figure 9. PDIP40 - 40 lead Plastic DIP, 600 mils width, Package Outline

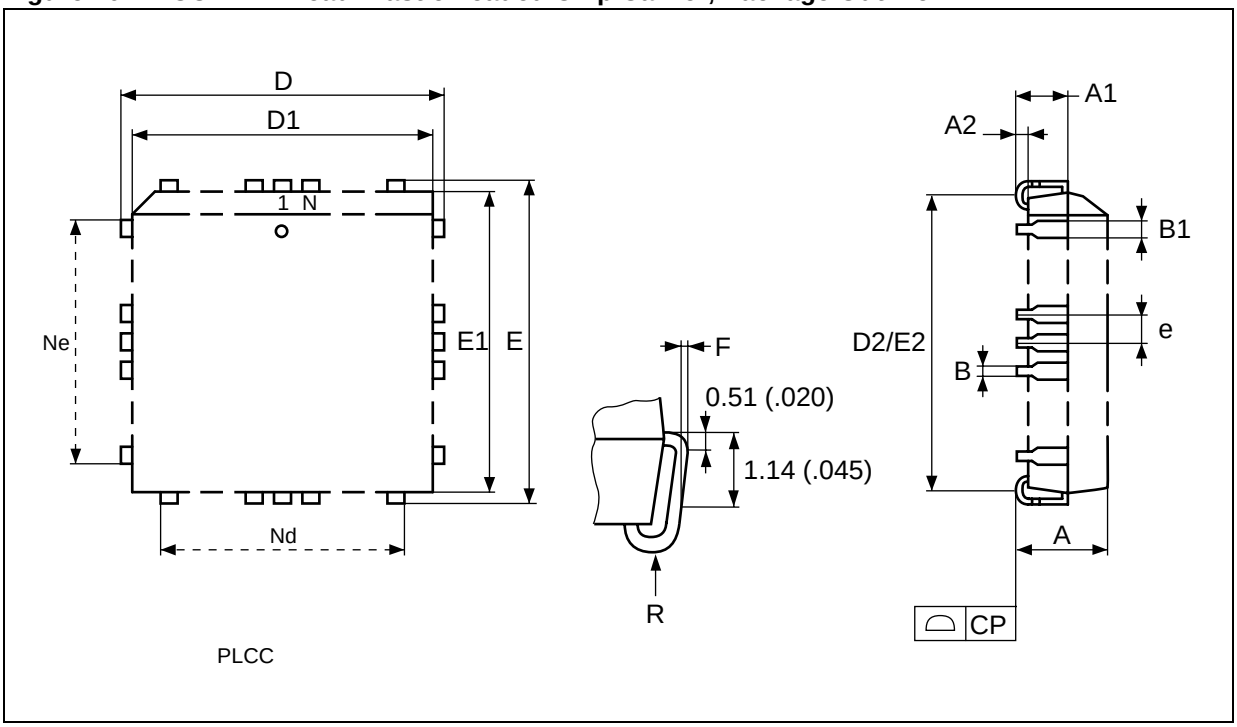


Drawing is not to scale.

Table 15. PLCC44 - 44 lead Plastic Leaded Chip Carrier, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
A2		–	0.51		–	0.020
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N		44			44	
CP			0.10			0.004

Figure 10. PLCC44 - 44 lead Plastic Leaded Chip Carrier, Package Outline

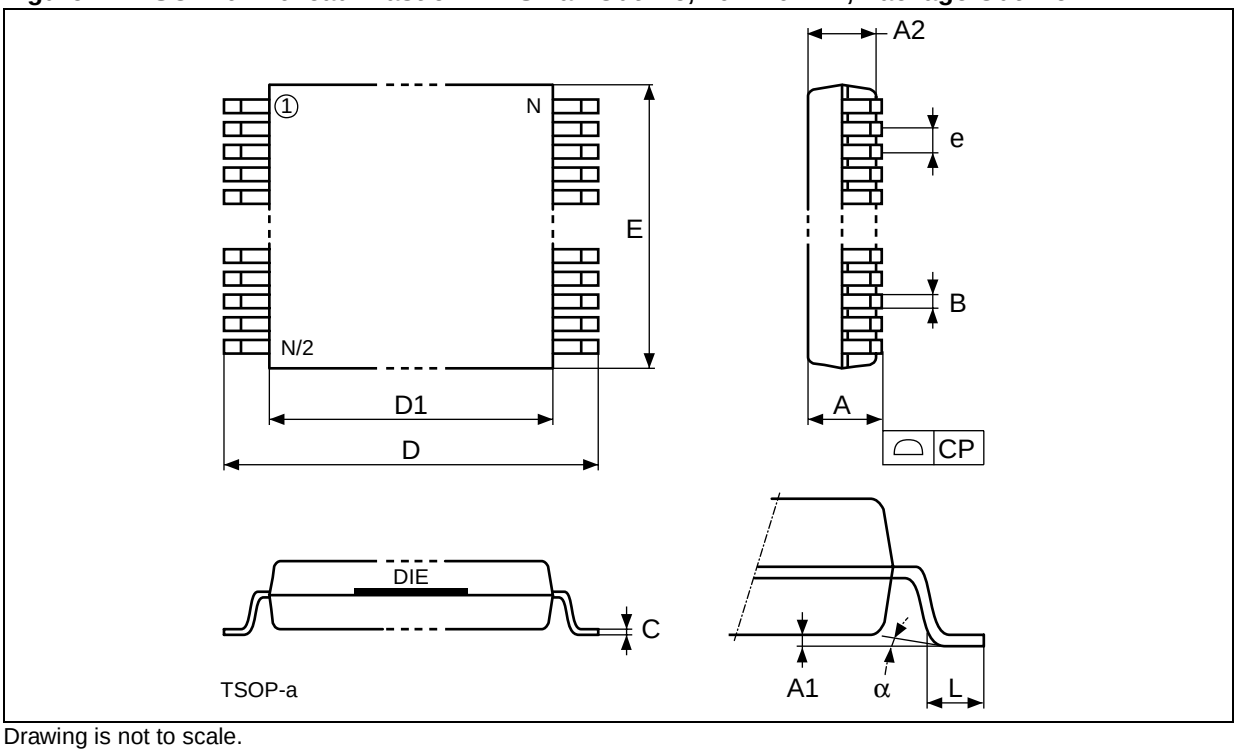


Drawing is not to scale.

Table 16. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20 mm, Package Mechanical Data

		mm			inch	
Symbol	**Typ**	**Min**	**Max**	**Typ**	**Min**	**Max**
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
B		0.170	0.270		0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
D		19.800	20.200		0.7795	0.7953
D1		18.300	18.500		0.7205	0.7283
e	0.500	–	–	0.0197	–	–
E		9.900	10.100		0.3898	0.3976
L		0.500	0.700		0.0197	0.0276
α		0°	5°		0°	5°
CP			0.100			0.0039
N	32			1.3		

Figure 11. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20 mm, Package Outline



Drawing is not to scale.

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